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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/849,047	05/04/2001	Gabriel Li	5298-04500	9067

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EXAMINER
LEWIS, MONICA

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/849,047	LI ET AL.	
	Examin r	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication app ars on th cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,17-21 and 23-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,17-21 and 23-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to the response filed April 28, 2003.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-11, 17-19 and 23-25 are rejected under 35 U.S.C. 103(a) as obvious over Wildi et al. (U.S. Patent No. 4,862,242) in view of Ikeda et al. (U.S. Patent No. 4,799,098).

In regards to claim 1, Wildi et al. ("Wildi") discloses the following:

a) transistor (350) formed in a well region of a semiconductor substrate, wherein the well region and the semiconductor substrate are of the same conductivity type (For Example: See Figure 3); and

b) a buried layer (318) formed within the substrate below the well region, wherein the buried layer is of opposite conductivity type than the well region (For Example: See Figure 3).

In regards to claim 1, Wildi fails to disclose the following:

a) a buried layer includes a first portion underlying the transistor and a second portion spaced apart from and laterally surrounding the first portion.

However, Ikeda et al. ("Ikeda") discloses a buried layer with various portions (2, 2', 14 and 14') (For Example: See Figure 2 and Figure 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Wildi to include a buried layer with various portions as disclosed in Ikeda because it aids in increasing the speed of the device (For Example: See Abstract).

Additionally, since Wildi and Ikeda are both from the same field of endeavor, the purpose disclosed by Ikeda would have been recognized in the pertinent art of Wildi.

In regards to claim 2, Wildi discloses the following:

a) a doped annular region (314 and 316) of opposite conductivity type as the well region and extending past the well region to contact the second portion of the buried layer (For Example: See Figure 3).

In regards to claim 3, Wildi discloses the following:

a) the doped annular region laterally surrounds the transistor without surrounding other transistors of the integrated circuit (For Example: See Figure 3).

In regards to claim 4, Wildi fails to disclose the following:

a) first and second portions of the buried layer are separated by a distance of less than about 5 microns.

However, the applicant has not established the critical nature of the dimension of less than about 5 microns. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

In regards to claim 5, Wildi fails to disclose the following:

a) first and second portions of the buried layer are separated by a distance of approximately 1.2 microns.

However, the applicant has not established the critical nature of the dimension of approximately 1.2 microns. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that

the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

In regards to claim 6, Wildi discloses the following:

a) one or more contact diffusions (364) within the well region adapted for making contact to the well region (For Example: See Figure 3).

In regards to claim 7, Wildi discloses the following:

a) one or more contact diffusions comprises a contact diffusion laterally adjacent to and in contact with the source region (352) (For Example: See Figure 3).

In regards to claim 8, Wildi discloses the following:

a) one or more contact diffusions comprises an annular contact diffusion arranged laterally within the doped annular region and laterally surrounding the transistor (For Example: See Figure 3).

In regards to claim 9, Wildi discloses the following:

a) a contact (320) to the doped annular region (For Example: See Figure 3).

In regards to claim 10, Wildi fails to disclose the following:

a) metallization adapted to connect the well region and the doped annular region to opposite polarities of a supply voltage.

Although Wildi does not specifically disclose metallization connecting the well region and the doped annular region to opposite polarities of a supply voltage, the metallization of Wildi would have been able to connect the well region and the doped annular region to opposite polarities of a supply voltage.

In regards to claim 11, Wildi discloses the following:

a) an annular dielectric isolation region laterally surrounding the transistor (For Example: See Figure 3).

In regards to claim 17, Wildi discloses the following:

a) a transistor formed in a well region of a semiconductor substrate, wherein the well region is of the same conductivity type as the substrate (For Example: See Figure 3);

b) a buried layer formed within the substrate below the well region, wherein the buried layer is of opposite conductivity type than the well region (For Example: See Figure 3); and

c) a doped annular region extending through the well region to contact the buried layer, wherein the doped annular region is of the same conductivity type as the buried layer (For Example: See Figure 3).

In regards to claim 17, Wildi fails to disclose the following:

a) metallization adapted to connect the well region to one polarity of a supply voltage for the integrated circuit, while precluding connection of the doped annular region to the other polarity of the supply voltage.

Although Wildi does not specifically disclose metallization connecting the well region to one polarity of a supply voltage for the integrated circuit, while precluding connection of the doped annular region to the other polarity of the supply voltage, the metallization of Wildi would have been able to connect the well region to one polarity of a supply voltage for the integrated circuit, while precluding connection of the doped annular region to the other polarity of the supply voltage.

In regards to claim 18, Wildi fails to disclose the following:

a) the metallization is adapted to preclude connection of the doped annular region to any supply voltage of the integrated circuit.

Although Wildi does not specifically disclose metallization precluding a connection of the doped annular region to any supply voltage of the integrated circuit, the metallization of Wildi would have been able to preclude a connection of the doped annular region to any supply voltage of the integrated circuit.

In regards to claim 19, Wildi fails to disclose the following:

a) the metallization is adapted to connect the well region and doped annular region to the same polarity of the supply voltage.

Although Wildi does not specifically disclose metallization connecting the well region and doped annular region to the same polarity of the supply voltage, the metallization of Wildi would have been able to connect the well region and doped annular region to the same polarity of the supply voltage.

In regards to claim 23, Wildi discloses the following:

a) a depletion region bridging the separation between the first and second portions of the buried layer, during times in which the well region and the doped annular region are connected to said opposite polarities of the supply voltage (For Example: See Figure 3).

In regards to claim 24, Wildi discloses the following:

a) the depletion region bridges the separation at a lower end of the buried layer (For Example: See Figure 3).

In regards to claim 25, Wildi discloses the following:

a) the depletion region increases noise isolation between the well region and the substrate (For Example: See Figure 3).

4. Claims 12, 13, 20 and 21 are rejected under 35 U.S.C. 103(a) as obvious over Wildi et al. (U.S. Patent No. 4,862,242) in view of Watanabe et al. (U.S. Patent No. 6,051,868).

In regards to claims 12 and 20, Wildi fails to disclose the following:

a) transistor is an output transistor for the integrated circuit.

However, Watanabe et al. ("Watanabe") discloses an output transistor (For Example: See Column 5 Lines 20-34). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Wildi to include an output

transistor as disclosed in Watanabe because it aids in reducing crosstalk (For Example: See Abstract).

Additionally, since Wildi and Watanabe are both from the same field of endeavor, the purpose disclosed by Watanabe would have been recognized in the pertinent art of Wildi.

In regards to claims 13 and 21, Wildi fails to disclose the following:

a) one or more analog circuit portions.

However, Watanabe discloses an analog circuit (For Example: See Column 2 Lines 32-37). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Wildi to include an analog circuit as disclosed in Watanabe because it aids in reducing crosstalk (For Example: See Abstract).

Additionally, since Wildi and Watanabe are both from the same field of endeavor, the purpose disclosed by Watanabe would have been recognized in the pertinent art of Wildi.

Response to Arguments

5. Applicant's arguments filed April 28, 2003 have been fully considered but they are not persuasive. First, Applicant argues that "Ikeda does not teach or suggest a buried layer with a first portion and a second portion spaced apart and laterally surrounding the first portion." However, Ikeda does disclose a buried layer that includes a first portion underlying the transistor and a second portion spaced apart from and laterally surrounding the first portion (2, 2', 14 and 14') (For Example: See Figure 2 and Figure 7). Additionally, Applicant argues "that there is no motivation to combine Ikeda with Wildi." However, as stated above the motivation is because it aids in increasing the speed of the device (For Example: See Abstract). Finally, Applicant argues that "none of the cited art teaches or suggests a doped annular region extending through a

well region." However, Wildi does disclose a doped annular region that extends through the well region (For Example: See Figure 3).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
July 7, 2003

AMIR ZARABIAN
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